

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		09989762
	Filing Date		2001-11-19
	First Named Inventor	Kenneth Y. Ogami	
	Art Unit	2123	
	Examiner Name	Osborne, Luke R.	
	Attorney Docket Number	CYPD-CD01175M	

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	4	6592626		2003-07-15	Bauchot , et al.		
	5	6611952		2003-08-26	Prakash , et al.		
	6	6613098		2003-09-02	Sorge , et al.		
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9	6715132		2004-03-30	Bartz , et al.	
10	6724220		2004-04-20	Snyder , et al.	
11	6792584		2004-09-14	Eneboe , et al.	
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13	6825869		2004-11-30	Bang	
14	6895373		2005-05-17	Garcia , et al.	
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2	20020188910	A1	2002-12-12	Zizzo, Claudio	
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	3	0499383	EP	A2	1992-08-19	ACTEL CORP		<input type="checkbox"/>
	4	1170671	EP	A1	2002-01-09	ST MICROELECTRONICS SRL		<input type="checkbox"/>
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	1	Kory Hopkins, "DEFINITION", 01/16/97, http://www.cs.sfu.ca/cs/people/GradStudent/sonal/papers/graph_isomorphism/node2.html	<input type="checkbox"/>

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2	C. Ebeling et al., "VALIDATING VLSI CIRCUIT LAYOUT BY WIRELIST COMPARISON"; Sept. 1983, In proceedings of the IEEE International Conference on Computer Aided Design (ICCAD-83), pp. 172-173	<input type="checkbox"/>
3	"THE GEMINI NETLIST COMPARISON PROJECT"; http://www.cs.washington.edu/research/projects/lis/www/gemini/gemini.html , larry@cs.washington.edu	<input type="checkbox"/>
4	Ohlrich et al., "SUB-GEMINI: IDENTIFYING SUBCIRCUITS USING A FAST SUBGRAPH ISOMORPHISM ALGORITHM"; June 1993, In proceedings of the 30th IEEE/ACM Design Automation Conference	<input type="checkbox"/>
5	Ebeling, "GEMINI II: A SECOND GENERATION LAYOUT VALIDATION PROGRAM"; 1988; In proceedings of the IEEE International Conference on Computer Aided Design (ICCAD-88), pp. 322-325	<input type="checkbox"/>
6	CYPR-CD00169; "PROGRAMMABLE MICROCONTROLLER ARCHITECTURE (MIXEDANALOG/DIGITAL)"; 08/07/01; 09/924,734; Snyder et al.	<input type="checkbox"/>
7	CYPR-CD00170; "DIGITAL CONFIGURABLE MACRO ARCHITECTURE"; 07/18/01; 09/909,045; W. Snyder	<input type="checkbox"/>
8	CYPR-CD00172; "CONFIGURING DIGITAL FUNCTIONS IN A DIGITAL CONFIGURABLE MACRO ARCHITECTURE"; 07/18/01; 09/909,109; W. Snyder	<input type="checkbox"/>
9	CYPR-CD00173; "A PROGRAMMABLE ANALOG SYSTEM ARCHITECTURE (AS AMENDED)"; 07/18/01; 09/909,047; M. Mar	<input type="checkbox"/>
10	CYPR-CD00174; "PROGRAMMING METHODOLOGY AND ARCHITECTURE FOR A PROGRAMMABLE ANALOG SYSTEM (AS AMENDED)"; 08/14/01; 09/930,021; Mar et al.	<input type="checkbox"/>
11	CYPR-CD00175; "METHOD FOR SYNCHRONIZING AND RESETTING CLOCK SIGNALS SUPPLIED TO MULTIPLE PROGRAMMABLE ANALOG BLOCKS (AS AMENDED)"; 10/01/01; 09/969,311; B. Sullam	<input type="checkbox"/>
12	CYPR-CD00180; "METHOD AND APPARATUS FOR PROGRAMMING A FLASH MEMORY"; 06/05/01; 09/875,599; W. Snyder	<input type="checkbox"/>

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13	CYPR-CD00182, "IN-SYSTEM CHIP EMULATOR ARCHITECTURE", 10/10/01, 09/975,115, Snyder et al.	<input type="checkbox"/>
14	CYPR-CD00187, "A CONFIGURABLE INPUT/OUTPUT INTERFACE FOR A MICROCONTROLLER", 09/14/01, 09/953,423, Kutz et al.	<input type="checkbox"/>

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